What is Claimed is:

1. Apparatus for receiving and processing a clock data recovery (CDR) signal comprising:

reference clock signal processing circuitry that receives as input a reference clock signal and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal;

data recovery circuitry that receives as input the recovered clock signal and the CDR signal and is operative to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock information to recover data information in the CDR signal; and

control circuitry that receives as input a first signal and a second signal and is operative to control the reference clock signal processing circuitry and the data recovery circuitry.

2. The apparatus of claim 1 wherein the reference clock signal processing circuitry comprises a divider circuit that divides the recovered clock signal by a predetermined scale factor.

3. The apparatus of claim 2 wherein the reference clock signal processing circuitry further comprises:

a phase frequency detector that compares the phase and frequency of the reference clock signal and an output signal of the divider circuit, and outputs a signal indicative of whether the output

signal of the divider circuit should be speeded up or slowed down to better match the phase and frequency of the reference clock signal.

4. The apparatus of claim 3 wherein the reference clock signal processing circuitry further comprises:

a charge pump that receives as input the output signal of the phase frequency detector; and

a loop filter that receives as input the output of the charge pump to produce a voltage controlled oscillator current control signal.

5. The apparatus of claim 4 wherein the reference clock signal further comprises:

a voltage controlled oscillator that receives as input the voltage controlled oscillator current control signal and outputs the recovered clock signal that better matches the phase and frequency of the reference clock signal.

6. The apparatus of claim 3 wherein the reference clock signal processing circuitry further comprises:

a lock detector that receives as input the output signal of the phase frequency detector and outputs a signal indicative of whether a phase of the output signal of the divider circuit is similar to the phase of the reference clock signal.

7. The apparatus of claim 2 wherein the reference clock signal processing circuitry further comprises:

a parts per million detector operative to output a signal indicative of when a frequency

difference between the reference clock signal and an output signal of the divider circuit is within a predetermined frequency setting.

8. The apparatus of claim 7 wherein the predetermined frequency setting is dynamically adjustable.

9. The apparatus of claim 1 wherein the data recovery circuitry further comprises a phase detector that compares a phase of the recovered clock signal and the CDR signal and outputs a signal indicative of whether the recovered clock signal needs to be speeded up or slowed down to better match the phase of the CDR signal.

10. The apparatus of claim 9 wherein the data recovery circuitry further comprises:

a charge pump that receives as input the output signal of the phase detector; and

a loop filter that receives as input the output of the charge pump to produce a voltage controlled oscillator current control signal.

11. The apparatus of claim 10 wherein the data recovery circuitry further comprises a voltage controlled oscillator that receives as input the voltage controlled oscillator current control signal and outputs the recovered clock signal that better matches the phase of the CDR signal.

12. The apparatus of claim 1 wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry:

first, directs operation of the reference clock signal processing circuitry; and

second, directs operation of the data recovery circuitry in response to receiving an output signal from the reference clock signal processing circuitry indicating that the recovered clock signal has a phase and frequency similar to the phase and frequency of the reference clock signal.

13. The apparatus of claim 1 wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry directs operation of the reference clock signal processing circuitry.

14. The apparatus of claim 1 wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry directs operation of the data recovery circuitry.

15. The apparatus of claim 1 wherein the first signal and the second signal are set by at least one of programmable logic resource core circuitry, circuitry external to programmable logic resource core circuitry, or user input.

16. A digital processing system comprising:

processing circuitry;

a memory coupled to the processing circuitry; and

apparatus as defined in claim 1 coupled to the processing circuitry and the memory.

17. A printed circuit board on which is mounted the apparatus as defined in claim 1.

18. The printed circuit board defined in claim 17 further comprising:

a memory mounted on the printed circuit board and coupled to the apparatus.

19. The printed circuit board defined in claim 17 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the apparatus.

20. Apparatus for receiving and processing a clock data recovery (CDR) signal comprising:

reference clock signal processing circuitry that receives as input a reference clock signal and is operative to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal;

data recovery circuitry that receives as input the recovered clock signal and the CDR signal and is operative to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock information to recover data information in the CDR signal;

a dynamically adjustable parts per million (PPM) detector operative to output a signal when a frequency difference between the reference clock signal and the recovered clock signal is within a predetermined frequency setting; and

control circuitry that receives as input

a first signal, a second signal, and the output signal of the PPM detector and is operative to control the reference clock signal processing circuitry and the data recovery circuitry.

21. The apparatus of claim 20 wherein the predetermined frequency setting is dynamically adjustable and set by at least one of programmable logic resource core circuitry, circuitry external to programmable logic resource core circuitry, or user input.

22. The apparatus of claim 20 wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry:

first, directs operation of the reference clock signal processing circuitry when the output signal of the PPM detector indicates that the frequency difference is not within the predetermined frequency setting; and

second, directs operation of the data recovery circuit when the output signal of the PPM detector indicates that the frequency difference is within the predetermined frequency setting.

23. The apparatus of claim 20 wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the control circuitry directs operation of the reference clock signal processing circuitry.

24. The apparatus of claim 20 wherein when the first signal is set to a first logic value and the second signal is set to a second logic value, the

control circuitry directs operation of the data recovery circuitry.

25. The apparatus of claim 20 wherein the first signal and the second signal are set by at least one of programmable logic resource core circuitry, circuitry external to programmable logic resource core circuitry, or user input.

26. A method for receiving and processing a clock data recovery (CDR) signal comprising:

receiving a reference clock signal and a CDR signal associated with a signaling protocol;

processing the reference clock signal and the CDR signal to recover data information from the CDR signal;

receiving a different reference clock signal and a different CDR signal associated with a different signaling protocol; and

processing the different reference clock signal and the different CDR signal to recover data information from the different CDR signal.

27. The method of claim 26 wherein processing the reference clock signal and the CDR signal comprises:

processing in reference clock mode to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal; and

processing in data mode to phase align the recovered clock signal to the CDR signal, to use the recovered clock signal to recover clock information embedded in the CDR signal, and to use the clock

information to recover the data information in the CDR signal.

28. The method of claim 27 wherein the processing in reference clock mode and the processing in data mode are controlled by a first signal and a second signal.

29. The method of claim 28 further comprising automatically switching from processing in reference clock mode to processing in data mode when the first signal is set to a first logic value, when the second signal is set to a second logic value, and when a frequency difference between the reference clock signal and the recovered clock signal is within a predetermined frequency setting.

30. The method of claim 29 wherein the predetermined frequency setting is dynamically adjustable.

31. The method of claim 28 further comprising automatically switching from processing in data mode to processing in reference clock mode when the first signal is set to a first logic value, when the second signal is set to a second logic value, and when a problem is detected during the processing in data mode.

32. The method of claim 28 further comprising processing in reference clock mode when the first signal is set to a first logic value and the second signal is set to a second logic value.

33. The method of claim 28 further comprising processing in data mode when the first signal is set to a first logic value and the second signal is set to a second logic value.

34. The method of claim 26 wherein processing the different reference clock signal and the different CDR signal comprises:

processing in reference clock mode to produce a recovered clock signal having a phase and frequency which respectively corresponds to a phase and frequency of the reference clock signal; and

processing in data mode to phase align the recovered clock signal to the different CDR signal, to use the recovered clock signal to recover clock information embedded in the different CDR signal, and to use the clock information to recover the data information in the different CDR signal.